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update

## VARIABLE FIXED MULTIPLIERS USING MEMORY BLOCKS

### PRIORITY INFORMATION

[0001] The present application is a continuation-in-part of commonly owned U.S. patent application serial no. 10/326,652 for Programmable Logic Device with Soft Multiplier filed 12/20/2002. <sup>1</sup> is now a U.S. Patent 6,888,372

### BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to programmable logic devices (PLDs), and more particularly to implementing multipliers in PLD RAM blocks.

[0004] 2. Description of the Related Art

[0005] A PLD is a digital, user-configurable integrated circuit used to implement a custom logic function. For the purposes of this description, the term PLD encompasses any digital logic circuit configured by an end-user, and includes a programmable array logic array ("PLA"), a field programmable gate array ("FPGA"), and an erasable complex PLD. The basic building block of a PLD is a logic element ("LE"). A LE is capable of performing limited logic functions on a number of input variables. Conventional PLDs combine together multiple LEs through an array of programmable interconnects to facilitate implementation of both simple and complex logic functions.

[0006] U.S. Patent Nos. 5,550,782 and 6,249,143 and commonly assigned U.S. patent application, Serial No. 10/140,311, filed May 6, 2002, entitled, Multiple Size Memories in a Programmable Logic Device, which are expressly incorporated herein by this reference, disclose the distribution of both relatively large random access memory (RAM) blocks and numerous smaller RAM blocks throughout a single programmable logic device. For example, U.S. Patent No. 6,249,143 discloses smaller RAM blocks associated with groupings of LEs called logic array blocks (LABs). Each LAB includes an identical collection of multiple LEs, programmable

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EAST History

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BRS	1357	(ram adj block) or (ramdom adj access adj memory adj block)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	1774	(RAM adj block) or (ramdom adj access adj memory adj block)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	610	S58 and shift	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	0	S59 and (multi-bit adj adder)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	217	S59 and adder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	0	multi-bit adj calculation adj result	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	22296	calculation adj result	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
BRS	4	S61 and S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB